Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) An input buffer receiver comprising:

a buffer input portion for receiving an input signal, said buffer input portion comprising a bias node;

a large capacitor coupled between the bias node and a lower supply voltage for providing a coupling ratio between a capacitance value of said large capacitor and a capacitance value of a parasitic capacitor coupled between said bias node and a ground reference point is approximately equal to a unity value such that a biasing voltage at said biasing node follows said lower supply voltage to minimize effects of a ground noise signal between the lower supply voltage and the ground reference point; and

a buffer output portion in communication with the buffer input portion for producing an output signal.

2. (Previously Presented) The input buffer receiver of claim 1, wherein the buffer input portion which receives the input signal further comprises:

a first transistor of a first conductivity type having a source node to which the lower supply voltage is applied, a gate node to which a reference voltage is applied, and a drain node at which the biasing voltage is developed;

a second transistor of a second conductivity type having a drain node which is connected to the drain node of the first transistor, and a gate node at which the biasing voltage is developed, and a source node to which an upper supply voltage source is applied;

a third transistor of the second conductivity type having a drain node, a gate node at which the biasing voltage is developed, and a source node to which the upper supply voltage source is applied;

a fourth transistor of the first conductivity type having a source node to which the lower supply voltage is applied, a gate node to which the input signal is applied, and a drain node which is coupled to the drain of a fourth transistor and to an input node of the buffer output portion.

3. (Previously Presented) The input buffer receiver of claim 2, wherein the first and fourth transistors are NMOS transistors, and the second and third transistors are PMOS transistors.

4. (Previously Presented) The input buffer receiver of claim 2, wherein the large capacitor is connected between the sources of the first and fourth transistors of the buffer input portion and the gate of the second transistor of the buffer input portion.

5. (Previously Presented) The input buffer receiver of claim 2, wherein the gate of the second transistor is connected to its drain.

6. (Previously Presented) The input buffer receiver of claim 2, wherein the gate of the second transistor is connected to the drain of the first transistor.

7. (Previously Presented) The input buffer receiver of claim 2, wherein the gate of the second transistor is connected to the gate of the third transistor.

8. (Previously Presented) The input buffer receiver of claim 2, wherein the buffer output portion which produces the output signal comprises: a first inverter connected to the drain of the third transistor and the drain of the fourth transistor.

9. (Previously Presented) The input buffer receiver of claim 2, wherein the third transistor and the fourth transistor activate and deactivate almost simultaneously as determined by said input signal to minimize the effects of ground noise on a delay jitter factor of said input buffer.

10. (Previously Presented) The input buffer receiver of claim 1, wherein the large capacitor charge couples the bias node of the input buffer receiver to the lower supply voltage of the input buffer receiver and wherein a capacitance value of the large capacitor is selected by the formula:

$$\frac{\mathbf{CHC}}{\mathbf{Cp} + \mathbf{CHC}} \approx \mathbf{1}$$

where:

CHC is the capacitance value of the large capacitor, and

Cp is the capacitance value of the parasitic capacitor.

11. (Currently Amended) The input buffer receiver of claim 1, wherein the capacitance value of the large capacitor is chosen to be very large with respect to **[[a]]** said capacitance value of said parasitic capacitor and results in a quicker response time for the output signal.

12. (Currently Amended) An integrated circuit formed on a substrate comprising:

an input buffer receiver for receiving an input signal, said input buffer comprising:

a buffer input portion for receiving the input signal, said buffer input portion comprising a bias node;

a large capacitor coupled between the bias node and a lower supply voltage for providing a coupling ratio between a capacitance value said large capacitor and a capacitance value of a parasitic capacitor coupled between said bias node and a ground reference point is approximately equal to a unity value such that a biasing voltage at said biasing node follows said lower supply voltage to minimize effects of a ground noise signal between the lower supply voltage and the ground reference point ; and

a buffer output portion in communication with the buffer input portion for producing an output signal.

13. (Previously Presented) The integrated circuit of claim 12, wherein the buffer input portion of the input buffer receiver further comprises:

a first transistor of a first conductivity type having a source node to which the lower supply voltage is applied, a gate node to which a reference voltage is applied, and a drain node at which the biasing voltage is developed;

a second transistor of a second conductivity type having a drain node which is connected to the drain node of the first transistor, and a gate node at which the biasing voltage is developed, and a source node to which an upper supply voltage source is applied;

a third transistor of the second conductivity type having a drain node, a gate node at which the biasing voltage is developed, and a source node to which the upper supply voltage source is applied;

a fourth transistor of the first conductivity type having a source node to which the lower supply voltage is applied, a gate node to which an input signal is applied, and a drain node which is connected to the drain of a fourth transistor and to an input node of the buffer output portion.

14. (Previously Presented) The integrated circuit of claim 13, wherein the first and fourth transistors are NMOS transistors, and the second and third transistors are PMOS transistors.

15. (Previously Presented) The integrated circuit of claim 13, wherein the large capacitor is connected between the sources of the first and fourth transistors of the buffer input portion and the gate of the second transistor of the buffer input portion.

16. (Previously Presented) The integrated circuit of claim 13, wherein the gate of the second transistor is connected to its drain.

17. (Previously Presented) The integrated circuit of claim 13, wherein the gate of the second transistor is connected to the drain of the first transistor.

18. (Previously Presented) The integrated circuit of claim 13, wherein the gate of the second transistor is connected to the gate of the third transistor.

19. (Previously Presented) The integrated circuit of claim 13, wherein the buffer output portion which produces said output signal comprises: a first inverter connected to the drain of the third transistor and the drain of the fourth transistor.

20. (Previously Presented) The integrated circuit of claim 13, wherein the third transistor and the fourth transistor activate and deactivate almost

simultaneously as determined by said input signal to minimize the effects of ground noise on a delay jitter factor of said input buffer.

21. (Previously Presented) The integrated circuit of claim 12, wherein the large capacitor charge couples the bias node of the input buffer receiver to the lower supply voltage of the input buffer receiver and wherein a capacitance value of the large capacitor is selected by the formula:

$$\frac{\mathbf{CHC}}{\mathbf{Cp}+\mathbf{CHC}} \approx \mathbf{1}$$

where:

CHC is the capacitance value of the large capacitor, and

Cp is the capacitance value of the parasitic capacitor.

22. (Currently Amended) The integrated circuit of claim 12, wherein the capacitance value of the large capacitor is chosen to be very large with respect to **[[a]]** said capacitance value of said parasitic capacitor and results in a quicker response time for the output signal.

23. (Currently Amended) A method for minimizing effects of ground noise on an input buffer receiver comprising the steps of:

forming a buffer input portion for receiving an input signal on a substrate;

forming a bias node within said buffer input portion;

connecting a lower supply voltage to said buffer input portion;

forming a large capacitor coupled between the bias node and the lower supply voltage for providing a coupling ratio between a capacitance value of said large capacitor and a capacitance value of a parasitic capacitor coupled between said bias node and a ground reference point is approximately equal to a unity value such that a biasing voltage at said biasing node follows said lower supply voltage to minimize effects of said ground noise between the lower supply voltage and the ground reference point; and

forming a buffer output portion on said substrate in communication with the buffer input portion for producing an output signal.

24. (Previously Presented) The method of claim 23, wherein forming the buffer input portion further comprises the steps of:

forming a first transistor of a first conductivity type on said substrate;

applying the lower supply voltage to a source node of the first transistor;

applying a reference voltage to a gate node of the first transistor;

connecting a drain node of the first transistor to develop **[[as]]** a biasing voltage at said drain node;

forming a second transistor of a second conductivity type on said substrate;

connecting a drain node of the second transistor to the drain node of the first transistor;

connecting a gate node of the second transistor to the drain node of the first transistor for developing the biasing voltage; and

connecting a source node of the second transistor to an upper supply voltage;

forming a third transistor of the second conductivity type on said substrate;

connecting a gate node of the third transistor to the drain node of the first transistor for developing the biasing voltage;

connecting a source node of the third transistor to the upper supply voltage source;

forming a fourth transistor of the first conductivity type on said substrate;

connecting a source node of the fourth transistor to the lower supply voltage;

connecting a gate node of the fourth transistor to receive an input signal; and

connecting a drain node of the fourth transistor to a drain node of the third transistor and to an input node of the buffer output portion.

25. (Previously Presented) The method of claim 24, wherein the first and fourth transistors are NMOS transistors, and the second and third transistors are PMOS transistors.

26. (Previously Presented) The method of claim 24, wherein forming the large capacitor comprises the step of:

connecting said large capacitor between the sources of the first and fourth transistors of the buffer input portion and the gate of the second transistor of the buffer input portion.

27. (Previously Presented) The method of claim 24, wherein forming the buffer input portion further comprises the steps of:

connecting the gate of the second transistor to its drain.

28. (Previously Presented) The method of claim 24, wherein forming the buffer input portion further comprises the steps of:

connecting the gate of the second transistor to the gate of the third transistor.

29. (Previously Presented) The method of claim 24, wherein forming the buffer output portion which produces the output signal comprises the step of:

forming a first inverter on said substrate; and

connecting an input of said first inverter to the drain of the third transistor and the drain of the fourth transistor.

30. (Previously Presented) The method of claim 24, wherein the third transistor and the fourth transistor activate and deactivate almost simultaneously as determined by said input signal to minimize the effects of ground noise on a delay jitter factor of said input buffer.

31. (Previously Presented) The method of claim 23, wherein the large capacitor charge couples the bias node of the input buffer receiver to the lower supply voltage of the input buffer receiver and wherein a capacitance value of the large capacitor is selected by the formula:

$$\frac{CHC}{Cp + CHC} \approx 1$$

where:

CHC is the capacitance value of the large capacitor, and

Cp is the capacitance value of the parasitic capacitor.

32. (Currently Amended) The method of claim 23, wherein the capacitance value of the large capacitor is chosen to be very large with respect to **[[a]]** said capacitance value of said parasitic capacitor and results in a quicker response time for the output signal.

33. (Currently Amended) An apparatus for minimizing effects of ground noise ~~on~~ within an input buffer receiver, said apparatus comprising:

means for forming a buffer input portion for receiving an input signal on a substrate;

means for forming a bias node within said buffer input portion;

means for connecting ~~said~~ a lower supply voltage to said buffer input portion;

means for forming a large capacitor between the bias node and the lower supply voltage for providing a coupling ratio between a capacitance value of said large capacitor and a capacitance value of a parasitic capacitor coupled between said bias node and a ground reference point is approximately equal to a unity value such that a biasing voltage at said biasing node follows said lower supply voltage to minimize effects of said ground noise between the lower supply voltage and the ground reference point; and

means for forming a buffer output portion on said substrate in communication with the buffer input portion for producing an output signal.

34. (Previously Presented) The apparatus of claim 33, wherein forming the buffer input portion further comprises:

means for forming a first transistor of a first conductivity type on said substrate;

means for applying the lower supply voltage to a source node of the first transistor;

means for applying a reference voltage to a gate node of the first transistor;

means for connecting a drain node of the first transistor to develop as biasing voltage at said drain node;

means for forming a second transistor of a second conductivity type on said substrate;

means for connecting a drain node of the second transistor to the drain node of the first transistor;

means for connecting a gate node of the second transistor to the drain node of the first transistor for developing the biasing voltage; and

means for connecting a source node of the second transistor to an upper supply voltage;

means for forming a third transistor of the second conductivity type on said substrate;

means for connecting a gate node of the third transistor to the drain node of the first transistor for developing the biasing voltage;

means for connecting a source node of the third transistor to the upper supply voltage source;

means for forming a fourth transistor of the first conductivity type on said substrate;

means for connecting a source node of the fourth transistor to the lower supply voltage;

means for connecting a gate node of the fourth transistor to receive **[[an]]** said input signal; and

connecting a drain node of the fourth transistor to a drain node of the third transistor and to an input of the buffer output portion.

35. (Previously Presented) The apparatus of claim 34, wherein the first and fourth transistors are NMOS transistors, and the second and third transistors are PMOS transistors.

36. (Previously Presented) The apparatus of claim 34, wherein means for forming the large capacitor comprises:

means for connecting said large capacitor between the sources of the first and fourth transistors of the buffer input portion and the gate of the second transistor of the buffer input portion.

37. (Previously Presented) The apparatus of claim 34, wherein means for forming the buffer input portion further comprises:

means for connecting the gate of the second transistor to its drain.

38. (Previously Presented) The apparatus of claim 34, wherein means for forming the buffer input portion further comprises the steps of:

means for connecting the gate of the second transistor to the gate of the third transistor.

39. (Previously Presented) The apparatus of claim 34, wherein means for forming the buffer output portion which produces said output signal comprises:

means for forming a first inverter on said substrate; and

means for connecting an input of said first inverter to the drain of the third transistor and the drain of the fourth transistor.

40. (Previously Presented) The apparatus of claim 34, wherein the third transistor and the fourth transistor activate and deactivate almost simultaneously as determined by said input signal to minimize the effects of ground noise on a delay jitter factor of said input buffer.

41. (Previously Presented) The apparatus of claim 33, wherein the large capacitor charge couples the bias node of the input buffer receiver to the lower supply voltage of the input buffer receiver and wherein a capacitance value of the large capacitor is selected by the formula:

$$\frac{\mathbf{CHC}}{\mathbf{Cp} + \mathbf{CHC}} \approx \mathbf{1}$$

where:

CHC is the capacitance value of the large capacitor CHC, and

Cp is the capacitance value of the parasitic capacitor Cp.

42. (Currently Amended) The apparatus of claim 33, wherein the capacitance value of the large capacitor is chosen to be very large with respect to **[[a]]** said capacitance value of said parasitic capacitor and results in a quicker response time for the output signal.